

EAST Search History

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|-------|------|---|----------|------------------|---------|------------------|
| L5 | 19 | (program\$ adj transceive\$3).clm. | US-PGPUB | OR | ON | 2006/08/18 12:31 |
| L6 | 15 | (program\$ adj (switch\$4 with circuit\$4)).clm. | US-PGPUB | OR | ON | 2006/08/18 12:32 |
| L8 | 92 | (program\$ adj (a?D)).clm. | US-PGPUB | OR | ON | 2006/08/18 12:33 |
| L9 | 0 | (program\$ adj (a\$1D with convert\$4)).clm. | US-PGPUB | OR | ON | 2006/08/18 12:33 |
| L10 | 0 | (program\$ adj (fpaa)).clm. | US-PGPUB | OR | ON | 2006/08/18 12:42 |
| L11 | 45 | (block with diagram and ((configurabl\$4 program\$) and (hardware))).clm. | US-PGPUB | OR | ON | 2006/08/18 12:40 |
| L12 | 0 | (program\$ adj ((field with program\$ with analog with array) fpaa)).clm. | US-PGPUB | OR | ON | 2006/08/18 12:43 |



block diagram hardware architecture file pro

- 1998

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Scholar Results 1 - 10 of about 90 for block diagram hardware architecture file programmable transceiver.

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A programmable CDMA IF transceiver ASIC for wireless

communications - group of 2 »

L Philips, I Bolsens, H De Man, L IMEC - Custom Integrated Circuits Conference, 1995., Proceedings of ..., 1995 - [ieeexplore.ieee.org](#)

... **Transceiver** functionality The PMCM functional **block diagram** is shown ... IF is done in the upcon- verter **block**. ... optimiza- tions such as **hardware** sharing, retiming ...

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Integrated circuit technologies for wireless communications - group of 2 »

B Daneshrad - Personal, Indoor and Mobile Radio Communications, 1998. The ..., 1998 - [ieeexplore.ieee.org](#)

... rake receivers has dictated a different **hardware architecture**. ... mag- Page 4 / Register

File \ Data Arithmetic Unit Figure 5. **Block Diagram** of dual ...

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A function specific EPLD for the PS/2 Micro Channel Bus adapter

YF Chan, CY Hung, C Hsiao, P Wong, N Lee, C ... - Custom Integrated Circuits Conference, 1989., Proceedings of ..., 1989 - [ieeexplore.ieee.org](#)

... The EPB200I **architecture** is designed to provide all ... 3 EPB2001 **BLOCK DIAGRAM USER CONFIGURATION** EPRA technology ... ports to control specific **hardware** functions on ...

[Web Search](#)

Cheops: a reconfigurable data-flow system for video processing - group of 12 »

VM Bove Jr, JA Watlington - Circuits and Systems for Video Technology, IEEE Transactions ..., 1995 - [ieeexplore.ieee.org](#)

... are then embodied in specialized **hardware** provided with ... convolution, correlation, matrix algebra, **block** transforms, spatial ... 2. Highly simplified **diagram** of the ...

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VLSI implementation of digital receivers for paging and PCS - group of 2 »

R Subramanian, M Barberis, H Dawid, KJ Koch - Personal, Indoor and Mobile Radio Communications, 1997.' ..., 1997 - [ieeexplore.ieee.org](#)

... 2: The VLSI **Architecture** Exploration Space ... the design across a particular **hardware** software boundary. ... approach is to convert the **block diagram** description of ...

[Web Search](#)

Real-time OS based radar controller for multi-mode phased array radar system - group of 4 »

YC Hwang, DH Hong, YK Kwag - Radar 97 (Conf. Publ. No. 449), 1997 - [ieeexplore.ieee.org](#)

... **Hardware architecture** of the radar controller is shown in f ... Figure 5 shows a **block diagram** of main task ... composed of tracking filter, **file** management, interrupt ...

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Implementation of a wideband CDMA mobile communication testbed - group of 2 »

LC de Silva, Z Liu, WC Wong - Military Communications Conference, 1998. MILCOM 98. ..., 1998 - [ieeexplore.ieee.org](#)

... 3 Tx—our 591 Figure 2. **Block Diagram** of the ... Figure 3. **Architecture** of the ASTRA Development Board [2 ... filter, gain control and upconversion **hardware**, if an ...

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A low-power 128-tap digital adaptive equalizer for broadband modems - group of 2 »

CJ Nicol, P Larsson, K Azadet, JH O'Neill - Solid-State Circuits, IEEE Journal of, 1997 - ieeexplore.ieee.org

... The slicer **block diagram** is shown in Fig ... are mapped onto the positive to halve the comparison hardware. ... The log base-2 **block** is implemented by first extracting ...

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A real-time MPEG encoder using a **programmable processor** - group of 2 »

D Kim, J Young, S Milton, HJ Kim, Y Kim - Consumer Electronics, IEEE Transactions on, 1994 - ieeexplore.ieee.org

... UWGSP5 **Architecture** Figure 2 is a **block diagram** of the ... simulations of the UWGSP5 **architecture** through a combination of Verilog hardware description language ...

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AlphaServer 4100 cached processor module **architecture** and design - group of 8 »

MB Steinman, GJ Harris, A Koccev, VC Lamere, RD ... - Digital Technical Journal, 1996 - research.compaq.com

... In the **block diagram** shown in Figure 1, the microprocessor ... To speed up this process, a hardware data buffer ... registers can hold the entire cache **block** (512 bits ...

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